Low k Interlevel Dielectric Layer Fabrication Methods

A1

TECHNICAL FIELD

This invention relates to methods of forming low k interlevel dielectric layers.

BACKGROUND OF THE INVENTION

In methods of forming integrated circuits, it is frequently desired to electrically isolate components of the integrated circuits from one another with an insulative material. For example, conductive layers can be electrically isolated from one another by separating them with an insulating material. Insulating material received between two different elevation conductive or component layers is typically referred to as an interlevel dielectric material. Also, devices which extend into a semiconductive substrate can be electrically isolated from one another by insulative materials formed within the substrate between the components, such as for example, trench isolation regions.

One typical insulative material for isolating components of integrated circuits is silicon dioxide, which has a dielectric constant of about 4. Yet in many applications, it is desired to utilize insulative materials having dielectric constants lower than that of silicon dioxide to reduce parasitic capacitance from occurring between conductive components separated by the insulative material. Parasitic capacitance

reduction continues to have increasing importance in the semiconductor fabrication industry as device dimensions and component spacing continues to shrink. Closer spacing adversely effects parasitic capacitance.

Sub B1

One way of reducing the dielectric constant of certain inherently insulative materials is to provide some degree of carbon content therein. One example technique for doing so has recently been developed by Trikon Technology of Bristol, UK which they refer to as Flowfill^{tm} Technology. Where more carbon incorporation is desired, methylsilane in a gaseous form and H_2O_2 in a liquid form are separately introduced into a chamber, such as a parallel plate reaction chamber. A reaction between the methylsilane and H_2O_2 can be moderated by introduction of nitrogen into the reaction chamber. A wafer is provided within the chamber and ideally maintained at a suitable low temperature, such as 0° C, at an exemplary pressure of 1 Torr to achieve formation of a methylsilanol structure. Such structure/material condenses on the wafer surface. Although the reaction occurs in the gas phase, the deposited material is in the form of a viscus liquid which flows to fill small gaps on the wafer surface. In applications where deposition thickness increases, surface tension drives the deposited layer flat, thus forming a planarized layer over the substrate.

The liquid methylsilanol is converted to a silicon dioxide structure by a two-step process occurring in two separate chambers from that in which the silanol-type structure was deposited. First, planarization of

the liquid film is promoted by increasing the temperature to above 100° C, while maintaining the pressure at about 1 Torr, to result in solidification and formation of a polymer layer. Thereafter, the temperature is raised to approximately 450°C, while maintaining a pressure of about 1 Torr, to form $(CH_3)_xSiO_y$. The $(CH_3)_xSiO_y$ has a dielectric constant of less than or equal to about 3, and is accordingly less likely to be involved in parasitic capacitance than silicon dioxide and/or phosphorous doped silicon dioxide.

Nevertheless, it would be desirable to develop improved methods for reducing parasitic capacitance of interlevel dielectric layers which comprise carbon and regardless of the method of manufacture of such layers.

SUMMARY

The invention comprises methods of forming low k interlevel dielectric layers. In one implementation, a low k interlevel dielectric layer fabrication method includes providing a substrate having integrated circuitry at least partially formed thereon. An oxide comprising interlevel dielectric layer comprising carbon and having a dielectric constant no greater than 3.5 is formed over the substrate. After forming the carbon comprising dielectric layer, it is exposed to a plasma comprising oxygen effective to reduce the dielectric constant to below what it was prior to said exposing.

4

In one implementation, a low k interlevel dielectric layer fabrication method includes providing a substrate having integrated circuitry at least partially formed thereon. In a chamber, an interlevel dielectric layer comprising carbon and having a dielectric constant no greater than 3.5 is plasma enhanced chemical vapor deposited over the substrate at subatmospheric pressure. After forming the carbon comprising dielectric layer, it is exposed to a plasma comprising oxygen at a subatmospheric pressure effective to reduce the dielectric constant by at least 10% below what it was prior to said exposing. The exposing occurs without removing the substrate from the chamber between the depositing and the exposing, and pressure within the chamber is maintained at subatmospheric between the depositing and the exposing.

In one implementation, a low k interlevel dielectric layer fabrication method includes providing a substrate having integrated circuitry at least partially formed thereon. An interlevel dielectric layer comprising a compound having silicon bonded to both nitrogen and an organic material and having a dielectric constant no greater than 8.0 over is formed over the substrate. After forming the dielectric layer, it is exposed to a plasma comprising nitrogen effective to reduce the dielectric constant to below what it was prior to said exposing.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, an exemplary semiconductor wafer fragment or substrate in process is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Substrate 10 comprises a bulk monocrystalline silicon substrate 12 having trench isolation oxide regions 14 formed therein. Integrated circuitry is at least partially formed thereon in the illustrated example in the form of a pair of transistors 16 and 18. Transistors 16 and 18 can comprise conventional constructions, such as overlying layers of gate oxide, polysilicon and silicide. Insulative spacers 20 are formed adjacent transistor gates 16 and 18. Conductively doped diffusion regions 22, 24 and 26 are formed within substrate 12 and proximate gates 16 and 18.

Referring to Fig. 2 and in accordance with but one aspect of the invention, an interlevel dielectric layer 30 comprising carbon and having a dielectric constant no greater than 3.5 is formed over the Fig. 1 substrate where layer 30 comprises oxide material. Such layer might be formed by a number of methods. One example preferred method includes the Flowfill^{tm} technique referred to above, whereby the formed interlevel dielectric level comprises or ultimately consists essentially of $(CH_3)_xSiO_y$, where x ranges from 1 to 3, and y ranges from 0-2. Such provides but one example where the dielectric layer formed comprises silicon bonded to organic material. Other dielectric layers, as well as the same or other layers, fabricated by different methods are also contemplated.

By way of example only, example preferred alternate methods of producing an interlevel dielectric layer at this point in the process are now described. Such encompass methods of forming insulative materials comprising carbon, silicon and oxygen. In one example, a first gaseous

precursor compound comprising carbon and silicon is combined with a second gaseous precursor compound comprising oxygen to form a second compound comprising carbon, silicon and oxygen. The first compound can comprise, for example, $(CH_3)_ySiH_x$, wherein y is an integer of from 1 to 4 and x is an integer from 0 to 3. The second precursor compound is an oxygen-containing moiety that is preferably a "dry" compound (i.e., a compound that does not either contain water or decompose to form water), and can comprise, for example, N_2O, or an activated oxygen species (e.g., high energy O_2, monatomic oxygen, or oxygen radicals). Such provides but one example process whereby water formation is avoided. In one example, the oxygen-containing moiety is generated by exposing O_2 to ultra-violet light (a process which can generate, for example, activated oxygen species in the form of O_3). In another aspect, the oxygen-containing moiety is generated by exposing an oxygen-containing gas (e.g., O_3, O_2, N_2O, CO, or CO_2) to a plasma. The plasma can be within the reaction chamber or remote from the chamber (i.e., not in the chamber). In another example, a compound comprising silicon, carbon and oxygen is formed by reaction of SiH_4 with an organic compound comprising oxygen (e.g., CO or CO_2).

In a more specific example, methylsilane or trimethylsilane is combined with N_2O in a reaction chamber. A pressure within the chamber is maintained at from about 300 mTorr to about 30 Torr, and is preferably maintained at from about 1 Torr to about 10 Torr. An

exemplary reaction chamber comprises a spacing from about 400 mils to about 600 mils with methylsilane being flowed into the chamber at a rate from about 25 standard cubic centimeters per minute (sccm) to about 2000 sccm (preferably at from about 50 sccm to about 250 sccm). The N_2O is flowed into the reaction chamber at a rate from about 50 sccm to about 3000 sccm (preferably at a rate from about 100 sccm to about 1500 sccm, and more preferably at a rate of from about 500 sccm to about 1200 sccm), and, additionally, helium is flowed into the reaction chamber at a rate of about 500 sccm to about 5000 sccm (preferably from 1000 sccm to about 3000 sccm). A radio frequency (RF) power within the chamber is maintained at from about 50 watts to about 500 watts, and preferably from about 100 watts to about 200 watts. The semiconductor substrate (such as a monocrystalline silicon wafer) is provided within the chamber and maintained at a temperature from about 25°C to about 450°C.

The above-described processing forms $(CH_3)_xSiO_y$ over a substrate. The concentration of methyl groups within the $(CH_3)_xSiO_y$ is typically from about 10% to about 50% (mole percent), i.e., where x equals or ranges from about 1 to about 3, and y ranges from 0 to about 2. Alternately by way of example only, x can be from about 0.1 to about 1, i.e., the concentration of methyl groups can be from about 5% to about 50% molar. In a particular example, a plasma can be generated within the chamber at a RF power of from about 50 watts to about 500 watts (preferably from about 80 watts to about 200 watts).

Such describes but one example process of forming an interlevel dielectric layer, here by chemical vapor deposition with or without plasma in a chemical vapor deposition chamber. In but another considered example, a gaseous precursor compound is introduced into a chemical vapor deposition reaction chamber and subjected to a plasma treatment. A semiconductor substrate is provided in the chamber, and material comprising carbon and silicon is deposited from the plasma-treated precursor compound to over the substrate. After the material is deposited, it is exposed to an oxygen containing moiety and converted to a second material comprising silicon, carbon and oxygen.

In a more specific example, methylsilane is flowed into a reaction chamber at a pressure of from 300 mTorr to about 30 Torr (preferably from about 1 Torr to about 10 Torr) and subjected to a plasma formed at a power of from about 50 watts to about 500 watts (preferably from 100 watts to about 200 watts). A semiconductor substrate is provided in the reaction chamber and maintained at a temperature of about 0° C to about 600° C. The plasma treated methylsilane deposits a material comprising methyl groups and silicon over the substrate. The deposited material is then exposed to an oxygen-containing moiety to convert the material to $(CH_3)_xSiO_y$. Accordingly in this example from the oxygen exposure, a whole of the deposited dielectric layer is transformed from one base chemistry (i.e., that comprising a nondescript combination of methyl groups and silicon) to another base chemistry (i.e., $(CH_3)_xSiO_y$) by the oxygen exposure. The oxygen-containing

moiety is preferably in gaseous form, and can comprise, for example ozone, O_2 and/or N_2O. In particular embodiments, the oxygen-containing moiety is subjected to plasma, heat or ultra-violet light. The oxygen treatment preferably occurs at a pressure of from about 300 mTorr to about 1 atmosphere, with the deposited material being maintained at a temperature of from about 0° C to about 600°C during the oxygen treatment to convert the base chemistry to $(CH_3)_xSiO_y$.

The above-described processings are again only example preferred techniques of forming the preferred interlevel dielectric layer material comprising carbon, here in the form of CH_3, and here producing a preferred layer of $(CH_3)_xSiO_y$. Alternate interlevel dielectric materials comprising carbon are of course contemplated. Further and by way of example only, the deposited interlevel dielectric layer at this point in the process might comprise silicon atoms bonded to both organic material and nitrogen, for example as described below.

After forming carbon comprising dielectric layer 30, in but one aspect of the invention, such layer is exposed to a plasma comprising oxygen effective to reduce the dielectric constant to below what it was prior to said exposing. Preferably, the exposing is at subatmospheric pressure to reduce the dielectric constant by at least 10%, and even more preferably by at least 15%, below what it was prior to said exposing. In a most preferred embodiment, the method by which the interlevel dielectric layer is initially formed is by plasma enhanced chemical vapor deposition in a chamber, with the subsequent exposing

of the plasma occurring in subatmospheric pressure in the same chamber. Further, the substrate is preferably not removed from the chamber between the depositing and the exposing. Further, the pressure within the chamber is preferably maintained at subatmospheric between the depositing and the exposing. Further, the exposing is ideally effective to increase stability of the dielectric constant to variation from what the stability was prior to the exposing. Specifically, stability of the dielectric constant of interlevel dielectric materials can have a tendency to increase over time or when exposed to subsequent thermal processing of at least 400°C. Ideally, the exposing is also effective to increase the stability of the dielectric constant of such film.

Exemplary processing in accordance with the invention has been achieved whereby a predominately $(CH_3)_xSiO_y$ interlevel dielectric layer after the exposing had a dielectric constant reduced from 3.0 to about 2.5 or 2.0.

The preferred wafer surface temperature during the exposing is always less than or equal to 550°C, with the exposing also preferably being conducted at subatmospheric pressure. The oxygen comprising plasma is preferably derived at least in part from at least one of O_2, O_3, N_2O, and NO_x. Preferred parameters for the exposing in a dual plate capacitively coupled reactor include an RF power range of from 300 to 1000 watts, a pressure range of from 1 Torr to 6 Torr, a temperature range of from 100°C to 450°C, a spacing between the plates of from 400 to 600 mils, an oxygen gas exposure flow of from

500 to 1500 sccm, an inert gas flow (i.e., He and/or Ar) of from 200 sccm to 800 sccm, and a treatment time of from 20 to 100 to more seconds. It is a preferred intent of the exposing to further not transform a whole of all of the dielectric layer from one base chemistry to another base chemistry by the exposing. An outermost portion of the exposed layer might experience a slight reduction in carbon content, but otherwise that portion and the whole of the layer is not transformed from one fundamental material to another even in spite of the low k reducing or resulting property. In one preferred aspect of the invention, the exposing comprises at least 20 seconds of processing time. More preferably and in preferred sequence, the processing comprises at least 40 seconds, 60 seconds, 80 seconds, and 100 seconds of oxygen containing plasma exposure. The plasma exposing is preferably ineffective to appreciably etch the interlevel dielectric layer.

Where the invention is conducted *in situ* in a plasma enhanced chemical vapor deposition chamber subsequent to the deposition, the exposing might comprise substantially ceasing feeding of one of the reactive gases while maintaining a feed of one of the precursors which comprises oxygen, and thereby maintaining plasma conditions from the deposition through an extended exposure time with the oxygen containing precursor to achieve the exposing effect.

In another considered aspect of the invention, a nitride comprising interlevel dielectric layer 30 is formed over the substrate to also comprise carbon and having a dielectric constant no greater than 8.0.

More preferred, interlevel dielectric layer 30 comprises a compound having silicon bonded to both nitrogen and an organic material and having a dielectric constant no greater than 8.0. After forming such dielectric layer, it is exposed to a plasma comprising nitrogen effective to reduce the dielectric constant to below what it was prior to said exposing, and preferably at least 15% below what it was prior to the exposing. By way of example only, a preferred deposited interlevel dielectric layer material comprises or consists essentially of $(CH_3)_xSi_3N_{(4-x)}$, wherein x is greater than 0 and no greater than 4. Such a composition can be formed by, for example, reacting inorganic silane with one or more of ammonia (NH_3), hydrazine (N_2H_4), or a combination of nitrogen (N_2) and hydrogen (H_2). The reaction can occur with or without plasma. However, if the reaction comprises an organic silane in combination with dinitrogen and dihydrogen, the reaction preferably occurs in the presence of plasma.

Sub B5

An exemplary specific reaction is to combine methylsilane (CH_3SiH_3) with NH_3 in the presence of a plasma to form $(CH_3)_xSi_3N_{(4-x)}$. The exemplary reaction can occur, for example, under the following conditions. A substrate if placed within a reaction chamber of a reactor, and a surface of the substrate is maintained at a temperature of from about 0°C to about 600°C. Ammonia and methyl silane are flowed into the reaction chamber, and a pressure within the chamber is maintained at from about 300 mTorr to about 30 Torr, with a plasma at a radio frequency (RF) power of from about

50 watts to about 500 watts. A product comprising $(CH_3)_xSi_3N_{(4-x)}$ is then formed and deposited on the substrate.

Using this particular described example, it was found that the product deposited from the described reaction consists essentially of $(CH_3)_xSi_3N_{(4-x)}$, (wherein x is generally about 1). The $(CH_3)_xSi_3N_{(4-x)}$ is present in the product to a concentration of from greater than 0% to about 50% (mole percent) and is preferably from about 10% to about 20%. The amount of $(CH_3)_xSi_3N_{(4-x)}$ present in the product can be adjusted by providing a feed gas of SiH_4 in the reactor in addition to the CH_3SiH_3, and by varying a ratio of the SiH_4 to the CH_3SiH_3, and/or by adjusting RF power.

The above provides but only one example of forming an interlevel dielectric layer comprising a compound having silicon bonded to both nitrogen and an organic material. Other methods of forming the same or different materials are of course contemplated.

After forming the dielectric layer, the nitrogen comprising plasma to which the layer is exposed preferably comprises one or more of N_2, NH_3, N_2H_4, N_2O, and NO_x. More preferably, the plasma exposing is preferably void of oxygen atoms therein. Wherein the dielectric layer is formed by chemical vapor deposition in a chamber, such as described above, the exposing preferably occurs within the chamber without removing the substrate from the chamber between the forming and the exposing. Again, the plasma exposing like in the first described

example is preferably conducted to be ineffective to appreciably etch the interlevel dielectric layer. Further, a whole of the dielectric layer subjected to the exposing is preferably not transformed from one base chemistry to another by the exposing. Preferred temperature, pressure, power, space arrangements, flows, and treatment times are as described above with respect to the first described embodiments.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.